



TOPSTAR TECHNOLOGY INDUSTRIAL CO., LIMITED

# 产 品 规 格 书

## *Product Specification Sheet*

**TOP-XEN-10G-SR**  
XENPAK 10GBASE-SR 850nm 300m Reach optical transceiver



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## **Features**

- Compatible with XENPAK MSA Rev.3.0
- Support of IEEE802.3ae up to 300m (OM3 MMF)
- Power Consumption 1.8W (typ.)
- Temperature Range 0 to 70°C
- Vertical Cavity Surface Emitting Laser at 850nm (VCSEL)
- Adaptable Power Supply (APS:+1.2V)
- SC duplex connector
- Hot pluggable 70-pin connector with XAUI electrical interface
- Management and control via MDIO 2-wire interface
- Compatible with RoHS

## **Applications**

- 10GBASE SR 10G Ethernet

## **Product Description**

The XENPAK Module is a highly integrated、Serial optical transponder module for high-speed, 10Gbit/s data transmission applications. 4×3.125Gbps Ethernet Signal Input by XAUI Interface.An integrated Coder / Decoder and multiplexer / demultiplexer (SERDES: Serializer / Deserializer). Designing for 10GBASE-SR Transmission with a Vertical Cavity Surface Emitting Laser at 850nm. The transponder operates within a wide case temperature range of 0°C to +70°C and offers optimum heat dissipation and excellent electromagnetic shielding which enables high port densities for 10 GbE systems. A 70 pin electrical connector and a duplex SC connector optical interface assure that connectivity is compliant to the XENPAK MSA Rev.3.0.

**Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit	Ref.
Storage Ambient Temperature Range		-40	+85	°C	
Powered case Temperature Range		0	+70	°C	
Supply Voltage APS	Vaps	0	1.5	V	
Supply Voltage Range @ 3.3V	Vcc3	-0.5	4.0	V	

Any stress beyond the maximum ratings can result in permanent damage. The device specifications are guaranteed only under the recommended operating conditions.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	Vcc3	3.13	3.3	3.47	V
	Vaps	1.152	1.2	1.248	
Power Dissipation	PD			2.2	W

**Electrical DC Characteristics**

(VCC3=3.14V to 3.47V, VCCaps=1.152V to 1.248V, Tc=0 to 70)						
Parameter	Symbol	min.	typ.	max.	Unit	
1.2V CMOS(1.8V CMOS Compatible1) I/O DC Characteristics (PRTAD; LASI; RESET; TX_ONOFF)						
Output High Voltage	Voh	1				V
Output Low Voltage	Vol			0.15		V
Input High Voltage	Vih	0.84		1.5		V
Input Low Voltage	Vil			0.36		V
Input Pull-down Current	Ipd	20		120		uA
XAUI I/O DC Characteristics (TXLANE[0..3]; RXLANE[0..3])						
Differential Input Amplitude (pk-pk) 4)		220		1600		mV
Differential Output Amplitude (pk-pk) 4)		800		1600		
MDIO I/O DC Characteristics (MDIO; MDC)						
Output Low Voltage	VOL	-0.3		0.2		V
Output Low Current	IOL			20		mA
Input High Voltage	VIH	0.84		1.5		V
Input Low Voltage	VIL	-0.3		0.36		V

1) For 1.8 V CMOS Voh = 1.65 V min., Vol = 0.15 V max., Vih = 1.17 V min., Vil = 0.63 V max.

2) Rpull-up = 10 kΩ to 1.8 V.

3) Vin = 1.8 V.

4) AC coupled



### Electrical AC Characteridtics

(VCC3 = 3.14 V to 3.47 V, VCC aps = 1.152 V to 1.248 V, TC = 0°C to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit
<b>XAUI Input AC Characteristics (TXLANE[0..3])</b>					
XAUI Baud Rate	DRin		3.125		Gbit/s
Differential Input Impedance	ZIN	80	100	120	Ω
<b>XAUI Output AC Characteristics (RXLANE[0..3])</b>					
XAUI Baud Rate	DRout		3.125		Gbit/s
XAUI Eye Mask (far-end)	According to IEEE 802.3ae				
Output Differential Impedance	ZO	80	100	120	Ω
Total Jitter <sup>4)</sup>	TJXAUI			0.35	UI
Deterministic Jitter <sup>4)</sup>	DJXAUI			0.37	UI
<b>Power-On Reset AC Characteristics</b>					
Power-On Reset AC Characteristics	According to XENPAK MSA Issue 3.0, 2002-9-18				
<b>MDIO I/O AC Characteristics (MDIO; MDC)</b>					
MDIO Data Hold Time	t <sub>HOLD</sub>	10			ns
MDIO Data Setup Time	t <sub>SU</sub>	10			ns
Delay from MDC Rising Edge to MDIO Data Change	t <sub>DELAY</sub>			300	ns
MDC Clock Rate	f <sub>MAX</sub>			2.5	MHz

- 1) 100 MHz to 2.5 GHz
- 2) At crossing point
- 3) Per IEEE Std 802.3ae
- 4) At near-end, No pre-equalization, 1 UI = 320 ps.



### Optical Interface Operating Conditions

Parameter	Fiber Type	Modal Bandwidth(MHz*km)	Symbol	Max.	Units
Operating range	62.5μm MMF	160	Lop	26	m
	50μm MMF	400		66	
	50μm MMF	500		82	
	50μm MMF	2000		300	

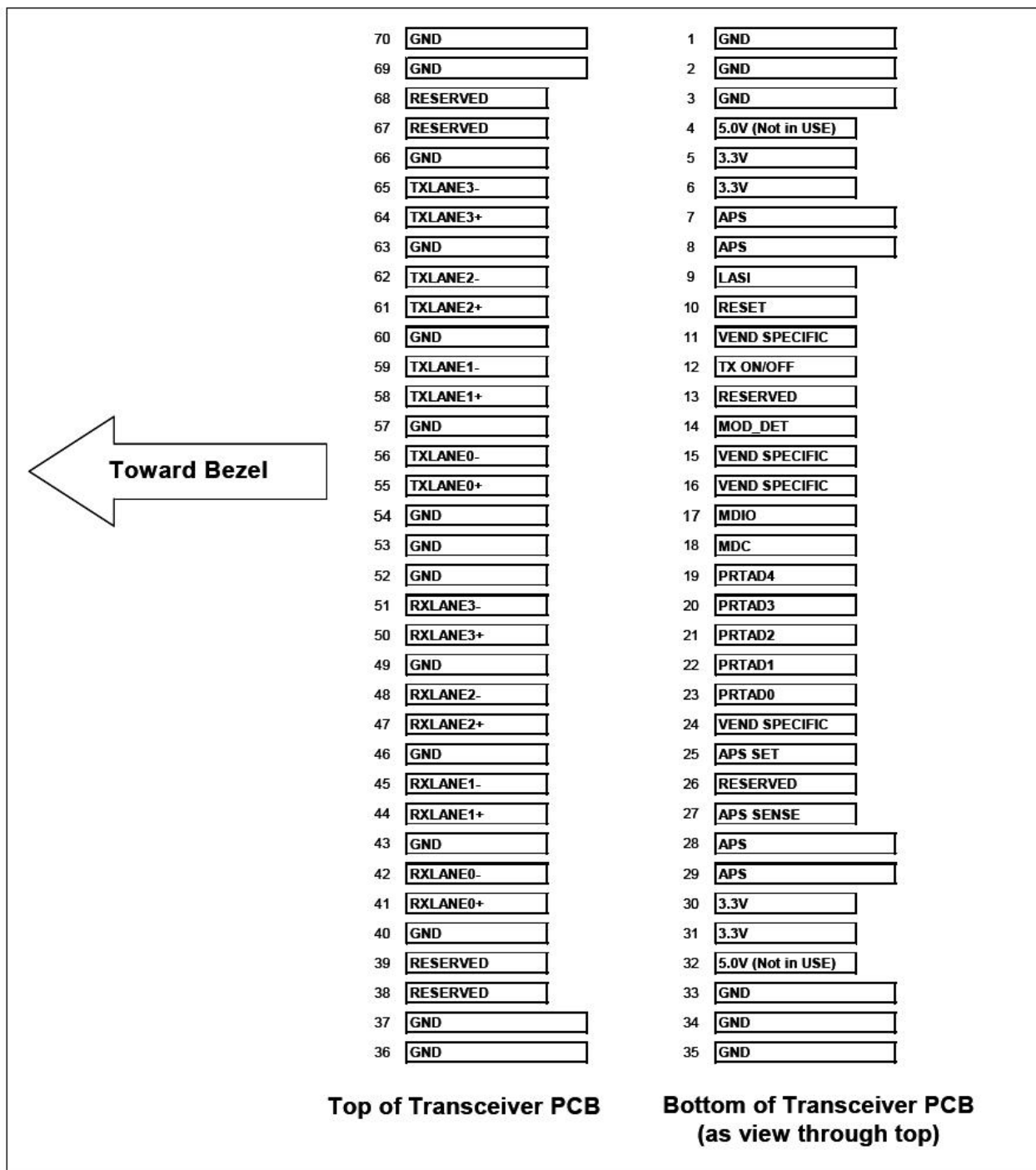
### Optical Characteristics

(VCC3 = 3.14 V to 3.47 V, VCC aps = 1.152 V to 1.248 V, TC = 0°C to 70°C, BER1E-12, Bit Rate 10.3125)					
Parameter	Symbol	min.	typ.	max.	Unit
<b>Transmitter</b>					
Average Launch Power	PAvg	-5		-1	dBm
Transmitter and Dispersion Penalty	TDP			3.9	dB
Center Wavelength Range1)	$\lambda$	840	850	860	nm
RMS Spectral Width1)	$\Delta\lambda$		0.4	0.45	nm
Extinction Ratio	ER	3.0			dB
Relative Intensity Noise <sup>2</sup> OMA	RIN			-128	dB/Hz
Eye Mask Definition	According to IEEE 802.3ae				
Optical Return Loss Tolerance	ORLT			12	dB
Average Launch Power of OFF Transmitter	Poff			-30	dBm
<b>Receiver</b>					
Stressed Receiver Sensitivity in OMA	Pssen			-7.5	dBm
Receiver Sensitivity in OMA <sup>2</sup> )	Psen			-11.1	dBm
Power Overload	Po			-1	dBm
Signal Detect Deassert Level	Psa			-14.0	dBm
Signal Detect Assert Level	PSD	-18			dBm
Signal Detect Hysteresis	PSD	0.5	1.5		dB
Center Wavelength Range	$\lambda$	840		860	nm

- 1) Conforms to IEEE triple trade-off between center wavelength, RMS spectral width and minimum OMA.
- 2) Receiver sensitivity, which is defined for an ideal input signal is informative only.



Electrical PAD Layout







### Host PCB XENPAK PINOUT

1	GND	GND	70
2	GND	GND	69
3	GND	RESERVED	68
4	5.0V (Not in USE)	RESERVED	67
5	3.3V	GND	66
6	3.3V	TXLANE3-	65
7	APS	TXLANE3+	64
8	APS	GND	63
9	LASI	TXLANE2-	62
10	RESET	TXLANE2+	61
11	VEND SPECIFIC	GND	60
12	TX ON/OFF	TXLANE1-	59
13	RESERVED	TXLANE1+	58
14	MOD_DET	GND	57
15	VEND SPECIFIC	TXLANE0-	56
16	VEND SPECIFIC	TXLANE0+	55
17	MDIO	GND	54
18	MDC	GND	53
19	PRTAD4	GND	52
20	PRTAD3	RXLANE3-	51
21	PRTAD2	RXLANE3+	50
22	PRTAD1	GND	49
23	PRTAD0	RXLANE2-	48
24	VEND SPECIFIC	RXLANE2+	47
25	APS SET	GND	46
26	RESERVED	RXLANE1-	45
27	APS SENSE	RXLANE1+	44
28	APS	GND	43
29	APS	RXLANE0-	42
30	3.3V	RXLANE0+	41
31	3.3V	GND	40
32	5.0V (Not in USE)	RESERVED	39
33	GND	RESERVED	38
34	GND	GND	37
35	GND	GND	36

**Pin Descriptions**

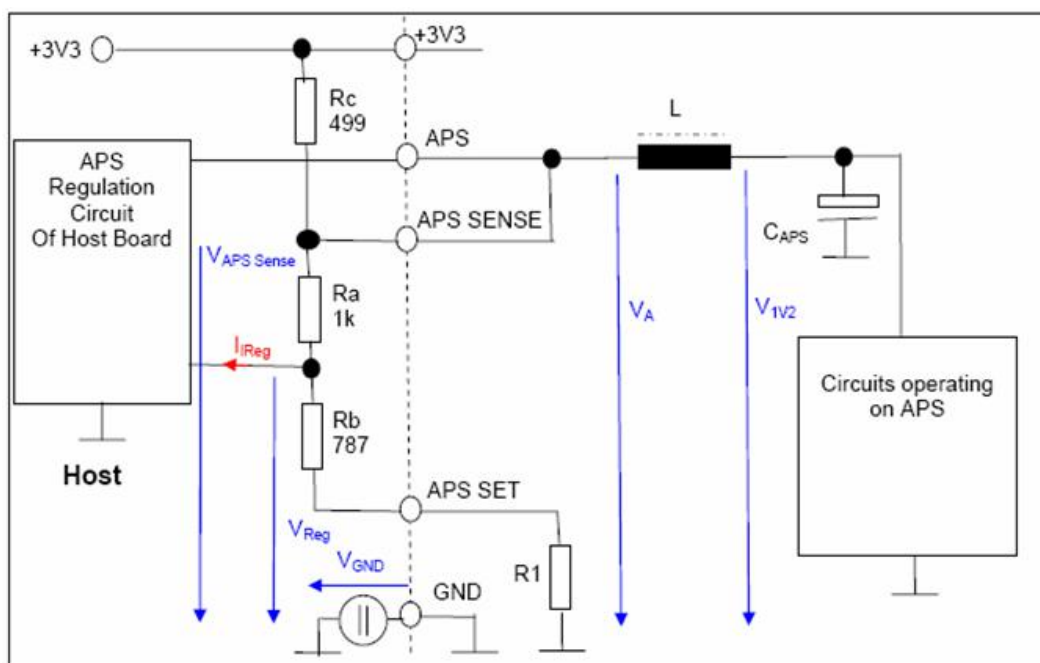
Signal Name	Level	I/O	Pin NO.	Description
GND			1,2,3,33,34,35,36,37,40,43,46,49,52,53,54,57,60,63,66,69,70	Ground connection for signal ground on the module
APS	+1.2V		7,8,28,29	Input from Adaptive Power Supply
APS SENSE	+1.2V		27	APS Sense Output. Connected to the APS Sense Output.Connected to the APS input from APS
APS SET			25	Feedback input from APS.Connected to GND through a 1.18Kohm resistor inside the transponder.
3.3V	+3.3 V DC		5,6,30,31	DC Power Input,+5.0 V DC,Nornimal
Reserved			25	Reserved for APD
Reserved			13	Reserved
MDIO	Open Drain	I/O	17	Management Data I/O.Requires external 10-22KΩ pull-up to the APS on host
MDC	1.2V CMOS	I	18	Management Data Clock Input
PRTAD4	1.2V CMOS	I	19	Port Address Input bit 4
PRTAD3	1.2V CMOS	I	20	Port Address Input bit 3
PRTAD2	1.2V CMOS	I	21	Port Address Input bit 2
PRTAD1	1.2V CMOS	I	22	Port Address Input bit 1
PRTAD0	1.2V CMOS	I	23	Port Address Input bit 0
LASI	Open Drain	O	9	Link Alarm Status Interrupt Output. Open Drain Compatible Output with 10 - 20 kΩ pull-up on host. Logic high = Normal Operation Logic low = Status Flag Triggered
RESET	Open Drain	I	10	Reset Input. Open Drain Compatible Input with 22 kΩ pull-up to APS internal to transponder. Logic high = Normal Operation Logic low = RESET
Vendor Specific			11,15,16,24	Vendor Specific Pins. Leave unconnected when not used.
TX ON/OFF	Open Drain	I	12	TX ON/OFF Input. Open Drain Compatible Input with 22 kΩ pull-up to APS internal to transponder. Logic high = Transmitter On Logic low = Transmitter Off
MOD DETECT		O	14	Pulled low inside transponder through a 1 kΩ resistor to Ground





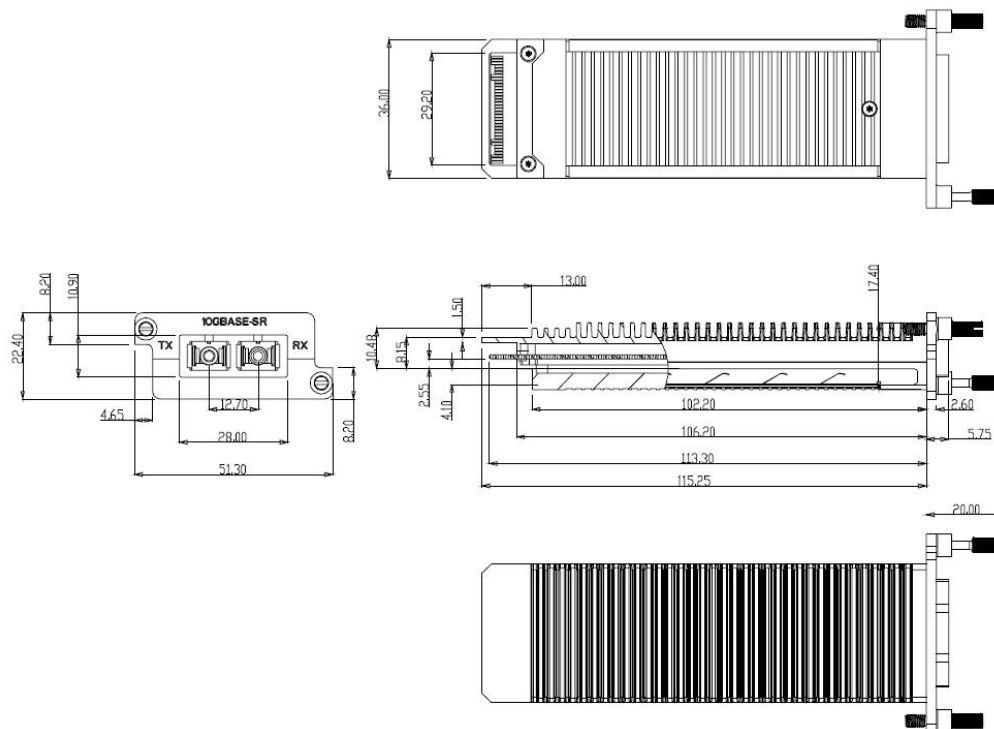
Reserved		I	67,68,38,39	Reserved For Future Use
TX LANE 3– TX LANE 3+		I	65 64	Module XAUI Input Lane 3– Module XAUI Input Lane 3+
TX LANE 2– TX LANE 2+		I	62 61	Module XAUI Input Lane 2– Module XAUI Input Lane 2+
TX LANE 1– TX LANE 1+		I	59 58	Module XAUI Input Lane 1– Module XAUI Input Lane 1+
TX LANE 0– TX LANE 0+		I	56 55	Module XAUI Input Lane 0– Module XAUI Input Lane 0+
RX LANE 0+ RX LANE 0–		O	41 42	Module XAUI Output Lane 0+ Module XAUI Output Lane 0–
RX LANE 1+ RX LANE 1–		O	44 45	Module XAUI Output Lane 1+ Module XAUI Output Lane 1–
RX LANE 2+ RX LANE 2–		O	47 48	Module XAUI Output Lane 2+ Module XAUI Output Lane 2–
RX LANE 3+ RX LANE 3–		O	50 51	Module XAUI Output Lane 3+ Module XAUI Output Lane 3–

**Block Diagram of Adapter Power Supply Circuit**





### Package Outline



### Ordering information

Part Number	Product Description
TOP-XEN-10G-SR	850nm, 10.3125Gbps, 300m(OM3 MMF), 0°C ~ +70°C



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